B' cont'd. surface and wherein the trench defines the distance between the device source and the device drain.

2. (unchanged) The semiconductor device of claim 1 wherein the distance between the spacers defines a device gate length.

3. (unchanged) The semiconductor device of claim 2 wherein the distance between the spacers is less than 50 nm.

REMARKS

This reply is in response to the Official Action mailed June 15, 2001. In that Official Action, the Examiner rejected applicants' claims 1 and 2 under 35 USC § 102(b). The Examiner cited the reference Chatterjee, A. et al., "CMOS Metal Replacement Gate Transistors using Tantalum Pentoxide Gate Insulator," IEDM 98, pp. 777-780 (1998) (Chatterjee et al. hereinafter) as the basis for the rejection. The Chatterjee et al. reference was cited by the applicants and is described on page 2, lines 6-13 of applicants' specification.

As noted by applicants, one of the problems with prior art sacrificial gates was the fact that the sacrificial gate itself was the fact that the sacrificial gate itself defines the distance between the source and the drain. This is readily observed in FIG. 1 a) of Chatterjee et al. Thus, Chatterjee et al. describes a device in which the distance between the source and drain is defined lithographically.

The difference between the device described in Chatterjee et al., and the device claimed by applicants, is readily observed with reference to FIG. 5 in applicants' specification. Specifically, the source and drain regions, 125 and 126 respectively, do not extend underneath the spacers 135. Claim 1 is amended to specifically recite the distance between the source and drain regions is defined by the trench. The advantages of using the replacement gate and spacers to define

the distance between the source and drain of the device is described on page 3, lines 4 to 28 of applicants' specification. Specifically, since the trench width is the combined gate length and spacer width, the lithographic requirements for defining the gate length are relaxed.

Chatterjee et al. does not disclose or suggest a device in which the combination of the distance between the source and drain is defined by the combination of the gate length and the spacer width. Since amended claim 1 requires that the trench defines the distance between the device source and drain (he trench width is defined by the replacement gate width and spacer width), Chatterjee et al. does not anticipate amended claim 1. Nor does Chatterjee et al. anticipate claim 2, which, though unamended, is patentable over Chatterjee et al. by virtue of its dependence on claim 1.

Nor does Chatterjee et al. render obvious applicants' invention under 35 U.S.C. § 103. As noted in applicants' specification, it is difficult to lithographically define device features with dimensions of less than 50 nm. In applicants' device, the device gate length is not defined lithographically. Instead, the trench width, which includes the gate length and spacer width, is defined lithographically. The sub lithographic gate length is defined by forming both the spacers and the gate in the trench. Furthermore, the advantage of abrupt dopant profile, discussed on page 2, lines 14-29 is not provided by Chatterjee's structure, nor is this advantage disclosed or suggested by Chatterjee et al.

The Examiner rejected claim 3 as obvious under 35 U.S.C. § 103(a). The Examiner again cited Chatterjee et al. as the basis for this rejection.

Claim 3 depends from amended claim 1. Amended claim 1 is patentable over Chatterjee et al. for the reasons that were previously stated. Hence claim 3 is also patentable over the Chatterjee et al. reference.

For the foregoing reasons, applicants submit that their amended claims are in condition for allowance. Favorable action from the Examiner is respectfully requested.

Any official fees associated with the entry and consideration of this Amendment may be charged to **Agere Systems Inc.** Deposit Account 501735.

Respectfully submitted,

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MARKED-UP VERSION OF AMENDED CLAIMS

1. (amended) A semiconductor device comprising:

a semiconductor substrate in which a source, drain and channel are formed;

a gate formed on a gate dielectric layer formed on the semiconductor substrate;

spacers adjacent to the gate wherein the gate and spacers are formed in a trench formed in a layer of dielectric material formed on the substrate surface and wherein the trench defines the distance between the device source and the device drain.

2. (unchanged) The semiconductor device of claim 1 wherein the distance between the spacers defines a device gate length.

3. (unchanged) The semiconductor device of claim 2 wherein the distance between the spacers is less than 50 nm.